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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,285	JOURDAN ET AL.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are pending in the instant application. The amendment after final submitted 12/19/2007 was entered on 7/19/2007 with the filing of a Request for Continued Examination. Applicant's arguments submitted 12/19/2006 have been carefully and fully considered, but are not persuasive.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 1-27** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. **Claim 1** has been amended to recite the limitation "by using bits of the full linear address to generate a lesser number of bits"

5. **Claims 2-10** depend from claim 1, and are rejected due to their dependence on claim 1.

6. **Claim 11** has been amended to recite the limitation "to generate a lesser number of bits"

7. **Claims 12-16** depend from claim 11, and are rejected due to their dependence from claim 11.

8. **Claim 17** has been amended to recite the limitation "said reduction module to use bits of the full linear address to generate a lesser number of bits for the reduced linear address"

9. **Claims 18-24** depend from claim 17, and are rejected due to their dependence on claim 17.

10. **Claim 25** has been amended to recite the limitation "said reduction module to use bits of the full linear address to generate a lesser number of bits for the reduced linear address"

11. **Claims 26 and 27** depend from claim 25, and are rejected due to their dependence from claim 25.

12. Each of these independent claims recite that bits of the full linear address are used "to generate a lesser number of bits". There is no indication what the number of bites is less than. Is it a lesser number of bits less than the number of bits in the full address, less than the number of bits of the full address used, or less than a different number of bits altogether?

13. The Examiner notes that the rejections under 35 USC 102(b) and 35 USC 103(a) infra are made in light of the rejections under 35 USC 112 second paragraph supra.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. **Claims 1-5, 11, 17-19, and 25-27** are rejected under 35 U.S.C. 102(b) as being anticipated by Doing et al. (US 6,161,166).

16. **Claim 1** is taught by Doing as:

a. *A method of processing addresses, comprising: receiving a full linear address of an instruction, and reducing a size of the full linear address to obtain a reduced linear address.* Column 10 lines 26-36 show that a hash function is used to convert the effective address to a 7 bit value.

b. *By using bits of the full linear address to generate a lesser number of bits.* Column 10 lines 26-35 shows that 7 bits of the effective address are used to generate a 7 bit hash function output. Accordingly, the hash function uses bits (bits 45-51) of the full linear address (64 bit effective address) to generate a lesser number of bits (7 is less than 64).

17. **Claim 2** is taught by Doing as:

c. *The method of claim 1, further including hashing a subset of the full linear address to reduce the size of the full linear address.* Column 10 lines 26-27 show that bits 45-51 of the effective address are used in the hash function.

18. **Claim 3** is taught by Doing as:

d. *The method of claim 2, wherein the full linear address includes one or more line offset bits and one or more set index bits, the method further including isolating the offset bits and the set index bits from the hashing.* Column 10 lines 26-27 show that only bits 45-51 of the effective address are used in the hash function, therefore isolating the offset and set index bits from the hashing.

19. **Claim 4** is taught by Doing as:

e. *The method of claim 2, further including hashing a thread signature with the subset of the full linear address.* The hash function shown in column 10 lines 34-35 includes the input ActT, which is shown in column 10 lines 31-32 to indicate which of the threads is active.

20. **Claim 5** is taught by Doing as:

f. *The method of claim 1, further including retrieving a data block from a data array if the reduced linear address corresponds to a tag in a tag array, the tag array being associated with the data array.* Column 10 lines 20-24 show that the ERAT contains a portion of the effective address, the tag, and a portion of a real address, a data block.

21. **Claim 11** is taught by Doing as:

g. *A method of retrieving data, comprising: receiving a full linear address of an instruction; reducing a size of the full linear address to obtain a reduced linear*

address to generate a lesser number of bits. Column 10 lines 26-35 shows that 7 bits of the effective address are used to generate a 7 bit hash function output. Accordingly, the hash function uses bits (bits 45-51) of the full linear address (64 bit effective address) to generate a lesser number of bits (7 is less than 64)

h. *The reducing including hashing a subset of the full linear address.* Column 10 lines 26-27 show that bits 45-51 of the effective address are used in the hash function.

i. *Isolating one or more cache line offset bits of the full linear address and one or more set index bits of the full linear address from the hashing.* Column 10 lines 26-27 show that only bits 45-51 of the effective address are used in the hash function, therefore isolating the offset and set index bits from the hashing.

j. *And retrieving a data block from a data array if the reduced linear address corresponds to a tag in a tag array, the tag array being associated with the data array.* Column 10 lines 20-24 show that the ERAT contains a portion of the effective address, the tag, and a portion of a real address, a data block.

22. **Claim 17** is taught by Doing as:

k. *An address processing unit comprising: a data structure having a data array and a tag array.* See figure 4A, which shows ERAT, item 301, containing a section for the effective address, the tag array, and a section for the real address, the data array.

l. *A reduction module to reduce a size of a full linear address of an instruction to obtain a reduced linear address.* Column 10 lines 26-36 show that a hash function is used to convert the effective address to a 7 bit value.

m. *Said reduction module to use bits of the full linear address to generate a lesser number of bits for the reduced linear address.* Column 10 lines 26-35 shows that 7 bits of the effective address are used to generate a 7 bit hash function output. Accordingly, the hash function uses bits (bits 45-51) of the full linear address (64 bit effective address) to generate a lesser number of bits (7 is less than 64)

n. *And a retrieval module to retrieve a data block from the data array if the reduced linear address corresponds to a tag in the tag array.* Column 10 lines 36-39 show that the appropriate ERAT entry is selected by select logic 401 of figure 4A in accordance with the hash function.

23. **Claim 18** is taught by Doing as:

o. *The address processing unit of claim 17, wherein the reduction module is to hash a subset of the full linear address to reduce the size of the full linear address.* Column 10 lines 26-27 show that bits 45-51 of the effective address are used in the hash function.

24. **Claim 19** is taught by Doing as:

p. *The address processing unit of claim 18, wherein the full linear address is to include one or more line offset bits and one or more set index bits, the reduction module to isolate the offset bits and the set index bits from the hashing.* Column 10 lines 26-27 show that only bits 45-51 of the effective address are used in the hash function, therefore isolating the offset and set index bits from the hashing.

25. **Claim 25** is taught by Doing as:

q. *A computer system comprising: a random access memory.* Figure 1A item 102.

r. *A bus coupled to the memory.* Figure 1A item 109

s. *And a processor coupled to the bus, the processor to receive an instruction from the memory and including an address processing unit having a data structure, a reduction module and a retrieval module.* Figure 1A item 101. CPU 101 is shown to contain I-cache 106. I-cache 106 is shown in column 8 lines 3-4 to contain ERAT 301. ERAT 301 contains a data structure, a reduction module, and a retrieval module.

t. *The data structure having a data array and a tag array.* Figure 4A shows ERAT 301, which contains a section for the effective address, the tag array, and a section for the real address, the data array.

u. *The reduction module to reduce a size of a full linear address of the instruction to obtain a reduced linear address.* Column 10 lines 26-36 show that a hash function is used to convert the effective address to a 7 bit value.

v. *Said reduction module to use bits of the full linear address to generate a lesser number of bits for the reduced linear address.* Column 10 lines 26-35 shows that 7 bits of the effective address are used to generate a 7 bit hash function output. Accordingly, the hash function uses bits (bits 45-51) of the full linear address (64 bit effective address) to generate a lesser number of bits (7 is less than 64)

w. *The retrieval module to retrieve a data block from the data array if the reduced linear address corresponds to a tag in the tag array.* Column 10 lines 36-39 show that the appropriate ERAT entry is selected by select logic 401 of figure 4A in accordance with the hash function.

26. **Claim 26** is taught by Doing as:

x. *The computer system of claim 25, wherein the reduction module is to hash a subset of the full linear address to reduce the size of the full linear address.* Column 10 lines 26-27 show that bits 45-51 of the effective address are used in the hash function.

27. **Claim 27** is taught by Doing as:

y. *The computer system of claim 26, wherein the full linear address is to include one or more line offset bits and one or more set index bits, the reduction module to isolate the offset bits and the set index bits from the hashing.* Column 10 lines 26-27 show that only bits 45-51 of the effective address are used in the hash function, therefore isolating the offset and set index bits from the hashing.

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. **Claims 1-5, 11, 17-19, and 25-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Doing et al. (cited supra) in view of Main et al. (Data Structures and Other Objects Using C++).

30. The Examiner notes that the rejections presented under 35 USC 103(a) are made under a different interpretation of the limitations related to generating a lesser number of bits, discussed supra with respect to the rejections under 35 USC 112 second paragraph, than the rejection presented supra under 35 USC 102(b).

31. Claim 1 is taught by Doing as:

z. *A method of processing addresses, comprising: receiving a full linear address of an instruction, and reducing a size of the full linear address to obtain a*

reduced linear address. Column 10 lines 26-36 show that a hash function is used to convert the effective address to a 7 bit value, using 7 bits of the effective address.

32. Doing does not expressly teach using bits of the full linear address to generate a lesser number of bits than the bits of the full linear address used.

33. With respect to claim 1, Main teaches the use of hash functions. At the third paragraph, it is shown that a good hash function will distribute the key values through the index range of the array. This property is well known to one of ordinary skill in the art.

34. Column 10 lines 36-39 shows that the 7 bit output of the hash function shown is used as an index into the 128 entries in the ERAT, this is clear to one of ordinary skill in the art, as 2^7 = 128.

35. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a 64 entry ERAT, which, as shown by Main and well known to one of ordinary skill in the art, would require a 6 bit output from the hash function, as 2^6 = 64.

36. The motivation for doing so would have been that a smaller ERAT would require less circuitry, as there would be half as many entries, which would require less chip space and therefore cost less.

37. Therefore, it would have been obvious to one of ordinary skill in the art to use bits of the full linear address to generate a lesser number of bits than the number of bits of the full linear address used to obtain the invention as recited in claims 1-5, 11, 17-19, and 25-27.

38. **Claim 2** is taught by Doing as:

aa. *The method of claim 1, further including hashing a subset of the full linear address to reduce the size of the full linear address.* Column 10 lines 26-27 show that bits 45-51 of the effective address are used in the hash function.

39. **Claim 3** is taught by Doing as:

bb. *The method of claim 2, wherein the full linear address includes one or more line offset bits and one or more set index bits, the method further including isolating the offset bits and the set index bits from the hashing.* Column 10 lines 26-27 show that only bits 45-51 of the effective address are used in the hash function, therefore isolating the offset and set index bits from the hashing.

40. **Claim 4** is taught by Doing as:

cc. *The method of claim 2, further including hashing a thread signature with the subset of the full linear address.* The hash function shown in column 10 lines 34-35 includes the input ActT, which is shown in column 10 lines 31-32 to indicate which of the threads is active.

41. **Claim 5** is taught by Doing as:

dd. *The method of claim 1, further including retrieving a data block from a data array if the reduced linear address corresponds to a tag in a tag array, the tag*

array being associated with the data array. Column 10 lines 20-24 show that the ERAT contains a portion of the effective address, the tag, and a portion of a real address, a data block.

42. **Claim 11** is taught by Doing and Main as: as:

ee. *A method of retrieving data, comprising: receiving a full linear address of an instruction; reducing a size of the full linear address to obtain a reduced linear address to generate a lesser number of bits*. Doing column 10 lines 26-35 shows that 7 bits of the effective address are used to generate a 7 bit hash function output. Main teaches that a number of bits can be hashed to a smaller number of bits, see the Introduction to Hashing on pages 545-546.

ff. *The reducing including hashing a subset of the full linear address*. Doing column 10 lines 26-27 show that bits 45-51 of the effective address are used in the hash function.

gg. *Isolating one or more cache line offset bits of the full linear address and one or more set index bits of the full linear address from the hashing*. Doing column 10 lines 26-27 show that only bits 45-51 of the effective address are used in the hash function, therefore isolating the offset and set index bits from the hashing.

hh. *And retrieving a data block from a data array if the reduced linear address corresponds to a tag in a tag array, the tag array being associated with the data*

array. Doing column 10 lines 20-24 show that the ERAT contains a portion of the effective address, the tag, and a portion of a real address, a data block.

43. **Claim 17** is taught by Doing and Main as:

ii. *An address processing unit comprising: a data structure having a data array and a tag array*. See figure 4A of Doing, which shows ERAT, item 301, containing a section for the effective address, the tag array, and a section for the real address, the data array.

jj. *A reduction module to reduce a size of a full linear address of an instruction to obtain a reduced linear address*. Doing column 10 lines 26-36 show that a hash function is used to convert the effective address to a 7 bit value.

kk. *Said reduction module to use bits of the full linear address to generate a lesser number of bits for the reduced linear address*. Doing column 10 lines 26-35 shows that 7 bits of the effective address are used to generate a 7 bit hash function output. Main teaches that a number of bits can be hashed to a smaller number of bits, see the Introduction to Hashing on pages 545-546.

ll. *And a retrieval module to retrieve a data block from the data array if the reduced linear address corresponds to a tag in the tag array*. Doing column 10 lines 36-39 show that the appropriate ERAT entry is selected by select logic 401 of figure 4A in accordance with the hash function.

44. **Claim 18** is taught by Doing as:

mm. *The address processing unit of claim 17, wherein the reduction module is to hash a subset of the full linear address to reduce the size of the full linear address.* Column 10 lines 26-27 show that bits 45-51 of the effective address are used in the hash function.

45. **Claim 19** is taught by Doing as:

nn. *The address processing unit of claim 18, wherein the full linear address is to include one or more line offset bits and one or more set index bits, the reduction module to isolate the offset bits and the set index bits from the hashing.* Column 10 lines 26-27 show that only bits 45-51 of the effective address are used in the hash function, therefore isolating the offset and set index bits from the hashing.

46. **Claim 25** is taught by Doing and Main as:

oo. *A computer system comprising: a random access memory.* Figure 1A item 102 of Doing.

pp. *A bus coupled to the memory.* Figure 1A item 109 of Doing.

qq. *And a processor coupled to the bus, the processor to receive an instruction from the memory and including an address processing unit having a data structure, a reduction module and a retrieval module.* Figure 1A item 101 of Doing. CPU 101 is shown to contain I-cache 106. I-cache 106 is shown in

column 8 lines 3-4 to contain ERAT 301. ERAT 301 contains a data structure, a reduction module, and a retrieval module.

rr. *The data structure having a data array and a tag array.* Figure 4A of Doing shows ERAT 301, which contains a section for the effective address, the tag array, and a section for the real address, the data array.

ss. *The reduction module to reduce a size of a full linear address of the instruction to obtain a reduced linear address.* Doing column 10 lines 26-36 show that a hash function is used to convert the effective address to a 7 bit value.

tt. *Said reduction module to use bits of the full linear address to generate a lesser number of bits for the reduced linear address.* Doing column 10 lines 26-35 shows that 7 bits of the effective address are used to generate a 7 bit hash function output. Main teaches that a number of bits can be hashed to a smaller number of bits, see the Introduction to Hashing on pages 545-546.

uu. *The retrieval module to retrieve a data block from the data array if the reduced linear address corresponds to a tag in the tag array.* Doing column 10 lines 36-39 show that the appropriate ERAT entry is selected by select logic 401 of figure 4A in accordance with the hash function.

47. **Claim 26** is taught by Doing as:

vv. *The computer system of claim 25, wherein the reduction module is to hash a subset of the full linear address to reduce the size of the full linear address.*

Column 10 lines 26-27 show that bits 45-51 of the effective address are used in the hash function.

48. **Claim 27** is taught by Doing as:

ww. *The computer system of claim 26, wherein the full linear address is to include one or more line offset bits and one or more set index bits, the reduction module to isolate the offset bits and the set index bits from the hashing.* Column 10 lines 26-27 show that only bits 45-51 of the effective address are used in the hash function, therefore isolating the offset and set index bits from the hashing.

Allowable Subject Matter

49. **Claims 6-10, 12-16, and 20-24** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

50. **Claims 6, 12, and 20** recite the limitation "wherein the data array is a prediction array of a branch predictor, the data block including a branch prediction address having a size that equals a size of the reduced linear address." The invention disclosed by Doing does not teach or suggest using a reduced linear address to locate a branch prediction address.

51. **Claims 7, 13, and 21** recite the limitation "wherein the data array is a cache array of a cache, the data block including a stored linear address having a size that equals the size of the full linear address." While the invention disclosed by Doing is a

cache, it only stores bits 0-46 of the effective address. Column 10 lines 42-46 state that is unnecessary to hold bits 47-51 because they were used in the hash function.

Response to Arguments

52. Applicant's arguments filed 12/19/2006 have been fully considered but they are considered moot in light of the new grounds of rejection presented supra.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jared I Rutz
Examiner
Art Unit 2187

jir

Brian R. Peugh
Primary Examiner
9/10/07